## AMENDMENTS TO THE SPECIFICATION

On p. 33, paragraph [00187]:

[00187] Each logic module contains configuration registers that can be read and written by an external processor using the Memory Emulation Interface. The Register Address Map is provided ~~in Section 3.2~~ below.

On p. 95, paragraph following Table 21:

Another Master Sequencer output, DemodFifoSelect, is used to specify which receive ~~Fifo~~ FIFO the word packer interfaces with as given by Table 22.

On p. 115, Abstract

Please replace the abstract with the following:

A system and method for processing UWB signals is implemented on an integrated circuit. The processing includes a plurality of rake teeth receiving a plurality of reflections of an impulse radio signal conveying unknown data, sampling the plurality of reflections, and determining a figure of merit for one or more of the plurality of reflections solely from samples of the corresponding one of the plurality of reflections. Samples of reflected signals may be excluded during demodulation based on the figure of merit. Rake teeth may be confined to a placement zone that may be adjusted based on the figure of merit. The energy of a rake tooth may be maximized based on the samples.